REMARKS

Applicants have carefully studied the Office Action of September 11, 2007 and offer the following remarks in response thereto.

Claim Rejection – 35 U.S.C. § 103(a)

Claims 1 and 40-83 presently stand rejected under 35 USC § 103(a) as allegedly unpatentable over U.S. Patent 6,643,689 B2 (Rode et al) in view of U.S. Patent 6,282,583 (Pincus et al). Without acquiescense in the grounds of rejection or prejudice to pursue at a later time, by continuation application or otherwise, independent claims 1, 52, 64, 72, and 75 have been amended to clarify the subject matter being claimed. This rejection is respectfully traversed.

Claims 1, 52, 64, and 72 are independent and will be addressed first, followed by independent claim 75, and finally the dependent claims.

Each of independent claims 1, 52, 64 and 72 generally relates in some manner to a "matrix" control network having (i) a plurality of control network data buses, and (ii) a supervisory network comprised of supervisory nodes and a physically distinct supervisory bus which collectively serve to, among other things, monitor the functioning of the control network. Because the hierarchical network involves multiple "data buses" that may be arranged in tiers, the use of a physically distinct "supervisory bus" can allow rapid, secure and reliable communication among the various supervisory nodes. In various embodiments, this architecture improves the speed of response of the supervisory network to problems that may occur in the control network being monitored or supervised, particularly at lower-tier buses (which could potentially be several layers removed from the top tier bus), and

also increases reliability as a failure of one control network data bus will not necessarily prevent the supervisory nodes from conveying events from the lower tiers fo the control network to the higher tiers in the control network being monitored. The specifics of the "matrix" control network are set forth in each of independent claims 1, 52, 64 and 72.

Turning to the specifics, claim 1 pertains to a "matrix control network" that, as amended, includes the following features:

1. A matrix control network, comprising:

a hierarchical control network, said hierarchical control network comprising a plurality of data buses arranged in a hierarchical structure, said data buses including a first-tier data bus and a plurality of lower-tier data buses;

a plurality of control network nodes arranged in a hierarchical structure according to their relative positioning in the hierarchy of data buses, each of said data buses communicatively coupling a plurality of said control network nodes; and

a supervisory network, said supervisory network comprising:

a supervisory communication bus physically distinct from the data buses;

a plurality of supervisory nodes communicatively coupled to said supervisory communication bus, said supervisory nodes including a plurality of supervisoring monitoring nodes each configured to monitor at least one of

the lower-tier data buses of said hierarchical control network, and at least one supervisory reporting node communicatively coupled to said first-tier data bus, whereby one or more control network nodes coupled to said first-tier data bus are apprised of events occurring on the lower-tier data buses.

Claim 1 thus includes, among other things, a "plurality of data buses" arranged in a "hierarchical structure" including a "first tier data bus" and a "plurality of lower-tier data buses," a "plurality of control network nodes arranged in a hierarchical structure according to their relative positioning in the hierarchy of data buses," and a "supervisory network" having a "supervisory communication bus" physically distinct from the data buses, and a "plurality of supervisory nodes" communicatively coupled to said supervisory communication bus. The supervisory nodes include a "plurality of supervisoring monitoring nodes each configured to monitor at least one of the lower-tier data buses of said hierarchical control network," and "at least one supervisory reporting node communicatively coupled to said first-tier data bus, whereby one or more control network nodes coupled to said first-tier data bus are apprised of events occurring on the lower-tier data buses."

Rode '689, by contrast, is concerned with forming different logical relationships among physical devices all connected to the same bus. Rode '689 does ***not*** involve, among other things, ***multiple data buses*** and, as a result, does not concern itself at all with the problems to which the matrix architecture of claim 1 is addressed. The need or desire for a physically distinct "supervisory bus" apart from the multiple data buses is not taught by Rode '689 and in fact, by using a

single bus to which all physical devices are connected, Rode '689 actually ***teaches away*** from the matrix architecture described in claim 1.

Newly cited Pincus '583 fails to teach the subject matter of claim 1 also. The Office Action asserts that Pincus '583 teaches a physically distinct supervisory communication bus, citing to Figures 7 and 9 and cols. 12:21-40 and 16:65 - 17:6 of Pincus '583, and concludes that "utilization of separate control and data buses is a commonplace technique that helps optimize data and control information distribution." However, the cited figures and text of Pincus '583 do not support the conclusions expressed in the Office Action. Figure 7 of Pincus '583 merely shows the wires of a ***single bus*** (referred to as "node bus 16" shown in Figs. 5A and 5B) divided into address/control lines (routed to a decoder 90) and data lines (fed to CPU registers 88) in order to transfer data to the appopriate register locations. The address/control lines do not constitute a separate "supervisory bus" which serve to allow a plurality of "supervisoring monitoring nodes" to monitor a plurality of "lower-tier data buses" of a hierarchical control network, as recited in claim 1.

Figure 9 of Pincus '583 shows a crossbar structure with incoming address/control lines and data lines for the purpose of "direct[ing] each data bus to the appropriate memory port 120 via the data lines 138." (See Col. 17, lines 4-6) This structure is merely a memory storage achitecture for routing data, and does not pertain to a "hierarchical control network" with a plurality of data buses in a "hierarchical configuration" and a distinct "supervisory communication bus." Nor does Pincus '583 teach a plurality of "supervisoring monitoring nodes" coupled to the supervisory communication bus, each configured to monitor at least one of the physically distinct lower-tier data buses of the hierarchical control network, along

with "at least one supervisory reporting node communicatively coupled to said first-tier data bus, whereby one or more control network nodes coupled to said first-tier data bus are apprised of events occurring on the lower-tier data buses," as recited in claim 1.

Since the essential features of claim 1 are lacking in both Rode '689 and Pincus '583, it follows that they are lacking in the proposed combination of these two patents as well. Moreover, it is unclear how or why the single-bus system of Rode '689 would be combined with the parallel address/data bus routing system of Pincus '583. Accordingly, it is respectfully submitted that claim 1 should be allowable over the two cited patents.

Claim 52 is a method claim having at least some analogous features to claim 1, including a "plurality of data buses" arranged "in a hierarchical structure" and including a "first-tier data bus and a plurality of lower-tier data buses," a plurality of control network nodes "arranged in a hierarchical structure according to their relative positioning in the hierarchy of data buses," and a "plurality of supervisory nodes" coupled to a "supervisory communication bus physically distinct from the data buses." Claim 52 further requires the steps of "monitoring communications over said data buses using said supervisory nodes," "communicating among said supervisory nodes over said supervisory communication bus according to a master-slave communication protocol," and "alerting one or more control network nodes coupled to said first-tier data bus of events occurring on the lower-tier data buses, via the supervisory nodes coupled to said supervisory bus." Again, neither Rode '689 nor Pincus '583 disclose or suggest a "plurality of data buses" arranged in a "hierarchical structure" as set forth in claim 52, nor a "plurality of supervisory nodes"

which are coupled to a "supervisory communication bus physically distinct from the data buses" and "monitor[] communications over said data buses." In addition, neither reference discloses or suggests such a control network which includes the further steps of "communicating among said supervisory nodes over said supervisory communication bus according to a master-slave communication protocol," and "alerting one or more control network nodes coupled to said first-tier data bus of events occurring on the lower-tier data buses, via the supervisory nodes coupled to said supervisory bus," all as required by claim 52.

Likewise, independent claim 64 relates to a "control network system" that includes, among other things, a "plurality of control network data buses arranged in a hierarchical structure ... including a first-tier data bus and a plurality of lower-tier data buses," a "plurality of control network nodes connected to said control network data buses," a "supervisory bus physically distinct from said network data buses," and a "plurality of supervisory nodes connected to said supervisory bus and to said control network data buses, said plurality of supervisory nodes configured to monitor said control network data buses and to alert one or more control network nodes coupled to said first-tier data bus of events occurring on the lower-tier data buses." It is respectfully submitted that Rode '689 and Pincus '583 fails to disclose or suggest an architecture as set forth in claim 64 for reasons described above.

Claim 72 relates to a "control network system" that includes, among other things, a "plurality of control network data buses connected to distinct sets of said nodes and arranged in a hierarchical structure, said plurality of control network data buses comprising a first-tier control network data bus and a plurality of lower-tier data buses," a "supervisory bus physically distinct from said network data buses,"

and a "plurality of supervisory monitoring nodes connected to said supervisory bus and to said lower-tier buses, each of said supervisory monitoring nodes configured to monitor one of said lower-tier buses." Claim 72 has been amended to further include "at least one supervisory reporting node communicatively coupled to said first-tier control network data bus and to said supervisory bus, whereby one or more control network nodes coupled to said first-tier control network data bus are apprised of events occurring on the lower-tier data buses via communications over said supervisory bus." It is respectfully submitted that Rode '689 and Pincus '583 fail to disclose or suggest an architecture having a "plurality of control network data buses" including a "first-tier control network data bus and a plurality of lower-tier data buses" arranged in a "hierarchical configuration" with corresponding network "nodes," along with a "supervisory bus physically distinct from said network data buses" with corresponding "supervisory monitoring nodes" arranged in the manner set forth in claim 72. It is also respectfully submitted that the two cited patents fail to disclose or suggest such an architecture further having "at least one a supervisory reporting node communicatively coupled to said first-tier control network data bus, whereby one or more control network nodes coupled to said first-tier control network data bus are apprised of events occurring on the lower-tier data buses via communications over said supervisory bus."

Accordingly, it is respectfully submitted that independent claims 1, 52, 64 and 72 are non-obvious and allowable over Rode '689 and Pincus '583.

Independent claim 75 involves a somewhat different configuration than those described in the other independent claims. Claim 75 relates to a "control network" including, among other things, a "first common bus" connecting a plurality of "first-

tier slave nodes in a loop configuration," a "physically distinct second common bus" connecting a plurality of "second-tier slave nodes in a loop configuration," with the second common bus connected to "at least one of said first-tier slave nodes functioning as a second-tier master node with respect to the second common bus," and a "first-tier master node connected to said first common bus, said first-tier master node comprising an uplink transceiver connected to said second common bus and a downlink transceiver connected to said first common bus." According to the unique arrangement of claim 75, a first-tier slave node acts as the "master" for the physically distinct second common bus, yet the first-tier master node that controls the slave nodes on the "first common bus" through commands issued via its "downlink transceiver" also comprises an "uplink transceiver" such that it can "listen" to activity on the "second common bus." This configuration may allow, for example, the first-tier master to directly monitor activity on the second physically distinct common bus, even though the first-tier master does not normally control the slave nodes on the second common bus. A failure of the second-tier master node on the second common bus can therefore be potentially determined very quickly by the first-tier master node.

It is respectfully submitted that, by contrast, Rode '689 does not disclose or suggest an architecture that includes, among other things, a "first common bus" connecting a plurality of "first-tier slave nodes" and a "second physically distinct common bus" connecting a plurality of "second-tier slave nodes," but rather only describe an architecture with a single physical bus 1 (see FIG. 1) which can support various *logical* arrangements (as detailed in the example of FIG. 2). It is further respectfully submitted that Rode '689 does not disclose or suggest an architecture

in which a plurality of "first-tier slave nodes" and a plurality of "second-tier slave nodes" are arranged in a "loop configuration" on a "first common bus" and "second common bus," respectively. Indeed, it does not appear that Rode et al '689 discusses a "loop configuration" at all. In addition, it is respectfully submitted that Rode '689 fails to disclose or suggest an arrangement in which a "first-tier master node" comprises an "uplink transceiver" connected to the "second common bus" thereby allowing it to, e.g., passively monitor activity occurring on the second common bus while at the same time controlling the first common bus as a "master" node. To make this operation more explicit, claim 75 has been amended to recite that the "uplink transceiver of said first-tier master node is configured to function as a second-tier slave node on said second common bus, thereby allowing said first-tier master node to monitor communications on said second common bus." It is respectfully submitted these features are not disclosed in either Rode '689 or Pincus '583, nor obvious in view thereof.

Claims 40-51, 53-63, 65-71, 73-74, and 76-83 depend, directly or indirectly, from independent claims 1, 52, 64, 72, 75 respectively. These claims should therefore be allowable at least because they depend from an allowable base claim. While additional novel and distinct features are believed to exist in the dependent claims, a detailed discussion thereof is not deemed necessary because of the differences between the independent claims and the two cited patents.

Reservation of Right to Challenge Cited Items

While Applicant has addressed the cited patents on the merits, this should not be construed as an admission that they constitute prior art as against the

claimed invention. Applicant reserves the right to antedate either of the cited patents pursuant to the appropriate rules, laws, and regulations if deemed necessary to do so.

Likewise, Applicant's election to address the cited patents on the merits should not be construed as an admission they provide an enabling disclosure. Applicant reserves the right to challenge the sufficiency of the cited patents at a later point in time, including in any post-issuance proceeding or suit, if appropriate.

Request for Allowance

The undersigned has made a good faith effort to respond to all of the rejections in the case and to place the claims in condition for immediate allowance. Nevertheless, if any unresolved issue remains, the Examiner is invited to contact the undersigned by telephone to discuss those issues so that the Notice of Allowance can be mailed at the earliest possible date.

It is believed that the instant application is in condition for final allowance, and, accordingly, issuance of a notice of allowance is earnestly solicited.

Respectfully submitted,

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Dated: February 11, 2008

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